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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,515	08/14/2001	Kumaraguru Muthukumaraswamy	K107-app	8393

7590 07/02/2003

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EXAMINER
CAO, CHUN

ART UNIT	PAPER NUMBER
2185	12

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/929,515	ROSTOKER ET AL.	
	Examiner	Art Unit	
	Chun Cao	2185	

-- The MAILING DATE of this communicati n appears n the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *23-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37,46 and 53* is/are allowed.

6)☒ Claim(s) *23-36,38-45,47-52 and 54-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 23-58 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Claims 23, 24, 26-28, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilson (Gilson), U.S. Patent No. 5,600,845 in view of Hansen et al. (Hansen), U.S. Patent No. 5,742,840.

Gilson is a prior art reference cited by applicant on paper no. 4.

As per claim 23, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip separately from the reconfigurable logic block for executing instructions [14, fig. 1; col. 5, lines 23-35; col. 6, lines 43-45, lines 60-61].

Gilson fails to disclose a block media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms.

Hansen discloses a media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms [fig. 7; col. 11, lines 52-60; col. 15, lines 7-21].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Hansen because Hansen's teachings of

implementing a variety of multimedia algorithms would improve the functionality of Gilson's system by allowing to execute virtual instructions.

As per claim 24, Gilson comprise an audio CODEC incorporated on the IC chip [90, 96, fig. 3; col. 8, lines 22-24, 48-50].

As per claims 26 and 47, inherently Gilson discloses a serial interface core and a configuration port that allow a user access to the block of reconfigurable logic from off-chip [providing input or output signal, col. 5, lines 45-50].

As per claim 27, Gilson discloses a CPU interface core [18, fig. 1; col. 5, line 26].

As per claim 28, Gilson discloses a memory interface core [fig. 1; col. 5, lines 32-33].

4. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilson, U.S. Patent No. 5,600,845 and Hansen et al. (Hansen), U.S. Patent No. 5,742,840 as applied to claim 1 above, and further in view of Chang (Chang), U.S. Patent No. 5,687,325.

Chang is a prior art reference cited by applicant in paper no. 4.

As per claim 25, Gilson and Hansen do not explicitly disclose a phase locked loop, such as a clock circuitry for synchronizing or delaying clock signal for the various blocks within the IC chip.

As per claims 24-28, Change discloses a video CODEC for interfacing to external analog signals [col. 7, lines 6-22]; a clock circuitry [62, fig. 2] for generating clock signal [col. 6, lines 40-41; col. 7, lines 24-25]; a serial interfacing core and a CPU interface core [col. 5, lines 8-10]; and a programmable memory interface core [col. 5, lines 19-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Hansen and Chang because Chang's teachings of having a clock circuitry would increase the reliability and efficiency of Gilson's system by allowing to reduce clock skew.

5. Claims 29, 31, 33-36, 38, 40, 42-45, 50, 52, 56, 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilson (Gilson), U.S. Patent No. 5,600,845 in view of Halahmi et al. (Halahmi), U.S. Patent No. 5,887,179.

6. As per claim 29, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

an audio CODEC incorporated on the IC chip for interfacing to external analog signals [90, 96, fig. 3; col. 8, lines 22-24, 48-50].

Gilson fails to disclose a power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the audio and/or video CODEC is not in use. In other word, Gilson fails to teach of using the power-down circuitry to power and/or processing savings when a portion of blocks (such as the audio and/or video CODEC) on the IC chip wherein the portion of blocks are not active.

Halahmi discloses a processor chip [col. 1, lines 27-29] having a power-down circuitry to power and/or processing savings when a portion of blocks [fig. 1, subsystems] on the IC chip [processor chip] wherein the portion of blocks are not active [col. 2, lines 14-22, 26-32, 56-61].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Halahmi because Halahmi's teachings of the power-down circuitry would improve the power consumption of Gilson's system by powering down the audio CODEC when it is not use.

7. As per claim 31, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

inherently Gilson discloses a fast serial interface core to interface to a serial interface standard incorporated on the IC chip [providing input or output signal, col. 5, lines 45-50].

Gilson fails to disclose a power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the serial interface core is not in use. In other word, Gilson fails to teach of using the power-down circuitry to power and/or processing savings when a portion of blocks (such as the serial interface core) on the IC chip wherein the portion of blocks are not active.

Halahmi discloses a processor chip [col. 1, lines 27-29] having a power-down circuitry to power and/or processing savings when a portion of blocks [fig. 1, subsystems] on the IC chip [processor chip] wherein the portion of blocks are not active [col. 2, lines 14-22, 26-32, 56-61].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Halahmi because Halahmi's teachings of the power-down circuitry would improve the power consumption of Gilson's system by powering down the

serial interface core when it is not use.

8. As per claim 33, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

a CPU interface core [18, fig. 1; col. 5, line 26].

Gilson fails to disclose a power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the CPU interface core is not in use. In other word, Gilson fails to teach of using the power-down circuitry to power and/or processing savings when a portion of blocks (such as the CPU interface core) on the IC chip wherein the portion of blocks are not active.

Halahmi discloses a processor chip [col. 1, lines 27-29] having a power-down circuitry to power and/or processing savings when a portion of blocks [fig. 1, subsystems] on the IC chip [processor chip] wherein the portion of blocks are not active [col. 2, lines 14-22, 26-32, 56-61].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Halahmi because Halahmi's teachings of the power-down circuitry would improve the power consumption of Gilson's system by powering down the

CPU interface core when it is not use.

As per claim 34, Gilson discloses the programmable CPU interface are incorporated within the reconfigurable logic block [fig. 1; col. 5, lines 29-35].

9. As per claim 35, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

a memory interface core [fig. 1; col. 5, lines 32-33].

Gilson fails to disclose a power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the memory interface core is not in use. In other word, Gilson fails to teach of using the power-down circuitry to power and/or processing savings when

a portion of blocks (such as the memory interface core) on the IC chip wherein the portion of blocks are not active.

Halahmi discloses a processor chip [col. 1, lines 27-29] having a power-down circuitry to power and/or processing savings when a portion of blocks [fig. 1, subsystems] on the IC chip [processor chip] wherein the portion of blocks are not active [col. 2, lines 14-22, 26-32, 56-61].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Halahmi because Halahmi's teachings of the power-down circuitry would improve the power consumption of Gilson's system by powering down the

memory interface core when it is not use.

As per claims 38 and 40, 42-44 are written in means plus function format and contain the same limitation as claims 29 and 31-35 respectively, therefore the same rejections applied.

As per claims 52 and 58 are written in means plus function format and contain the same limitation as claim 35, therefore the same rejections applied.

As per claims 36 and 45, Gilson discloses the programmable memory interface is incorporated within the reconfigurable logic block [fig. 1; col. 5, lines 29-35].

As per claims 50 and 56, Office notice is taken that the USB and IEEE-1394 interfaces are old and well-known type of bus interface in the computer art. It would have been obvious to one of ordinary skill in the art at the time of invention to implement Gilson's serial interface as USB and IEEE-1394 in order to provide fast data transfer.

10. Claims 30, 39, 49 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilson, U.S. Patent No. 5,600,845 in view of Chang (Chang), U.S. Patent No. 5,687,325 and Halahmi et al. (Halahmi), U.S. Patent No. 5,887,179.

As per claim 30, Gilson discloses a multimedia interface [fig. 1, 3; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

Gilson do not explicitly disclose a phase locked loop, such as a clock circuitry for synchronizing or delaying clock signal for the various blocks within the IC chip. Gilson further fails to disclose a power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the PLL circuitry is not in use. In other word, Gilson fails to teach of using the power-down circuitry to power and/or processing savings when a portion of blocks (such as the PLL circuitry) on the IC chip wherein the portion of blocks are not active.

Change discloses a clock circuitry [62, fig. 2] for generating clock signal [col. 6, lines 40-41; col. 7, lines 24-25].

Halahmi discloses a processor chip [col. 1, lines 27-29] having a power-down circuitry to power and/or processing savings when a portion of blocks [fig. 1, subsystems] on the IC chip [processor chip] wherein the portion of blocks are not active [col. 2, lines 14-22, 26-32, 56-61].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gilson and Chang and Halahmi because the specific teachings Chang and Halahmi stated above would increase the reliability and efficiency of Gilson's system by allowing to reduce clock skew and improve the power consumption of Gilson's system by powering down the PLL circuitry when it is not use.

As per claims 39 and 49 and 55 are written in means plus function format and contain the same limitation as claim 30, therefore the same rejections applied.

11. Claims 32, 41, 51 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilson (Gilson), U.S. Patent No. 5,600,845

as per claim 32, Gilson discloses an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC] incorporated on the IC chip [14, fig. 1; col. 5, lines 23-35];

inherently Gilson discloses a programmable, fast serial interface core to interface to a serial interface standard incorporated within the reconfigurable logic block [providing input or output signal, fig. 2, col. 5, lines 45-50].

As per claim 41 is written in means plus function format and contain the same limitation as claim 32, therefore the same rejections applied.

As per claims 51 and 57, Office notice is taken that the USB and IEEE-1394 interfaces are old and well-known type of bus interface in the computer art. It would have been obvious to

one of ordinary skill in the art at the time of invention to implement Gilson's serial interface as USB and IEEE-1394 in order to provide fast data transfer.

12. Claims 48 and 54 are rejected under 35 U.S.C. 102(e) as being anticipated by Gilson, U.S. Patent No. 5,600,845 (hereinafter "Gilson").

As claim 48, Gilson discloses a multimedia interface [fig. 1; col. 7, lines 53-56] comprising:

an integrated circuit chip [10, fig. 1; abstract, lines 1-3];

a block of reconfigurable logic as a field programmable gate array that incorporated on the chip [16, fig. 1; col. 5, lines 24-26];

a block media processor [RISC processor] incorporated on the chip separately from the reconfigurable logic block [14, fig. 1; col. 5, lines 23-35]; and

an audio CODEC and an analog interface incorporated on the IC chip, the audio CODEC communicating via the analog interface with external analog signal [90, 96, fig. 3; col. 8, lines 22-24, 48-50].

As per 54 is written in means plus function format and contain the same limitation as claim 48, therefore the same rejections applied.

Allowable Subject Matter

13. Claims 37, 46 and 53 are allow over prior art.

14. Applicant's arguments filed 4/24/2003 have been fully considered but are not persuasive in view of new ground(s) rejection.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any response to this action should be mailed to:

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Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703)308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703)305-9717. The fax number for this Art Unit are followings: After-Final (703) 746-7238; Official (703) 746-7239; Non-Official (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)306-5631.

Chun Cao

June 25, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100